Computer Architecture

Milestone III

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1. **Items updated from since Milestone 3**

* **Hazard Unit:**

Completely removed since stalling is no longer required and is accounted for by the fact that each 2 instructions happen in one clock cycle.

* **Flushing Unit:**

Modifications done:

* Removal of MUX that dictated whether the output of the instruction memory into the IF/ID register would be flushed or would resume normally. This was removed after the implementation of one memory since flushing at this stage was no longer required.
* **Registers:**
* Some of the registers were updated to accommodate more bits
  + **IF/ID** was increased to (96) bits for PC (32 bit), PC+4 (32 bit), and instruction/data (32 bit) .
  + **ID/EX** register was increased to (191) bits to account for the control signal (13) bits propagated PC+4 (32 bits), propagated PC (32 bits), ID\_EX\_readdata1\_input (32), immediate (32), rs1 (5), rs2(5), rd (5), func3 (3).
  + **EX/MEM** register was increased to (144) bits to account for the propagated control signals (7 bits), the result of the comparator (1 bit), the aluresult (32 bits), the muxb\_input (32 bits), the immediate(32), rd (5), func3(3), PC+4 (32),
  + **MEM/WB** register was updated to 104 bits to account for the propagated controls (3 bits), readdata(32 bits), the aluresult (32 bits), rd (5 bits) , PC+4 (32 bits).
* **Comparator:**
  + Was moved to the **EX**  stage in order to be able to assure that the rs1 and rs2 values that the comparator uses are chosen after the Forwarding MUXs and the source MUXs for the ALU. This ensures that the comparator sources are within the same stage in which the result of the comparator is produced.
* **Control unit:** 
  + One notable update in the control unit is the for the JAL which also now utilizes the Auipc control signal.
* Details of Control signals for the different instruction types, as well as the values of the multiplexers are given in the excel sheet.